CLAIMS:

1. A method of generating a random number sequence, particularly in a chip card or smart card, characterized by the steps of

(a) scanning the outputs of Nosz independent frequency oscillators and buffering corresponding Nosz output signals of the Nosz frequency oscillators at each clock of a clock signal from an external clock signal source,

(b) applying the buffered signals of step (a) to a logic operation assigning a predetermined output value to the Nosz buffered signals as input values,

(c) generating the parity of a predetermined number Nlog of output values of step (b) at each Nlogth clock of the external clock signal,

(d) storing a predetermined number Nz of parity numbers in a random-number register, and

(e) reading all of the Nz*Nlog clocks of the clock signal as a random number from the random-number register

2. A method as claimed in claim 1, characterized in that the frequency of at least one frequency oscillator is changed and/or modulated in dependence upon an MSB (Most Significant Bit) of a signature register.

3. A method as claimed in claim 2, characterized in that the frequency of the changed or modulated frequency oscillator is switched between > 20 MHz and > 40 MHz in dependence upon the MSB of the signature register.

4. A method as claimed in any one of the preceding claims, characterized in that the frequency of at least one frequency oscillator is selected to be > 30 MHz.

5. A method as claimed in any one of the preceding claims, characterized in that the frequency oscillators are voltage-controlled or current-controlled.

6. A method as claimed in any one of the preceding claims, characterized in that in step (a), the output signals of the two frequency oscillators are buffered in a respective flip-flop, particularly a delay flip-flop (D-F/F).

7. A method as claimed in any one of the preceding claims, characterized in that in step (c) the logic operation is an AND operation (AND), an OR operation (OR), a NOR operation (NOR), an Exclusive-OR operation (XOR), a NAND operation (NAND) or an Exclusive-NOR operation (XNOR).

8. A method as claimed in any one of the preceding claims, characterized in that the frequencies of the Nosz frequency oscillators are selected to be such that no frequency of a frequency oscillator is an integral multiple of another frequency oscillator or of the external clock signal.

9. A method as claimed in any one of the preceding claims, characterized in that Nosz is an integer which is larger than or equal to 1, particularly Nosz = 2.

10. A method as claimed in any one of the preceding claims, characterized in that Nlog and Nz are integers which are larger than or equal to 1.

11. A random-number generator, particularly for a chip card or a smart card, particularly for performing a method as claimed in any one of the preceding claims, characterized by a predetermined number Nosz of mutually independent frequency oscillators (10, 12), a predetermined number Nosz of flip-flops (14, 16), in which an output (26) of a frequency oscillator (10, 12) is connected to an input D (30) of a flip-flop (14, 16), a logic circuit element (18) receiving outputs Q (32) of the flip-flops (14, 16) as input values (36, 38) and, in accordance with a predetermined logic operation, assigns an output value (40) to these input values (36, 38), a parity circuit (20) determining the parity of a predetermined number Nlog of output values (40) from the logic circuit element (18), a random-number register (22) which buffers a predetermined number Nz of parity numbers (44) from the parity circuit (20) and supplies them as Nz bit random number, and an input (58) for an external clock signal source which clocks the flip-flops (14, 16), the parity circuit (20) and the random-number register (22).

12. A random-number generator as claimed in claim 11, characterized in that at least one frequency oscillator (10) is connected to an output of a signature register which applies an MSB (Most Significant Bit) (29) to the frequency oscillator, the frequency of the frequency oscillator (10) changing in dependence upon the MSB (29) of the signature register.

13. A random-number generator as claimed in claim 12, characterized in that the frequency oscillator (10) connected to the signature register is formed in such a way that it switches its frequency between > 20 MHz and > 40 MHz in dependence upon the MSB (29) of the signature register.

14. A random-number generator as claimed in any one of claims 11 to 13, characterized in that the frequency of at least one frequency oscillator (12) is > 30 MHz.

15. A random-number generator as claimed in any one of claims 11 to 14, characterized in that the frequency oscillators (10, 12) are formed as voltage-controlled or current-controlled frequency oscillators.

16. A random-number generator as claimed in any one of claims 11 to 15, characterized in that at least one flip-flop (14, 16) is formed as a delay flip-flop (D-F/F).

17. A random-number generator as claimed in any one of claims 11 to 16, characterized in that the logic circuit element (18) is an AND element (AND), an OR element (OR), a NOR element (NOR), an Exclusive-OR element (XOR), a NAND element (NAND) or an Exclusive-NOR element (XNOR).

18. A random-number generator as claimed in any one of claims 11 to 17, characterized in that the Nosz frequency oscillators (10, 12) are formed in such a way that no frequency of a frequency oscillator (10, 12) is an integral multiple of another frequency oscillator (10, 12) or of the external clock signal (58).

19. A random-number generator as claimed in any one of claims 11 to 18, characterized in that Nosz is an integer which is larger than or equal to 1, particularly Nosz = 2.

20. A random-number generator as claimed in any one of claims 11 to 19, characterized in that Nlog and Nz are integers which are larger than or equal to 1.

LIST OF REFERENCE SIGNS

10	frequency oscillator OSC1
12	frequency oscillator OSC1
14	delay flip-flop LATCH1
16	delay flip-flop LATCH2
18	logic circuit element XNOR
20	parity generator PARITY
22	random-number register REG
24	reset input RES of the frequency oscillator
26	output OUT of the frequency oscillator
28	additional input MOD for MSB of the frequency oscillator
29	SIGMSB
30	input D of the flip-flop
32	output Q of the flip-flop
34	clock input CL of the flip-flop
35	reset input RES of the flip-flop
36	input A of the logic circuit element
38	input B of the logic circuit element
40	output OUT of the logic circuit element
42	input IN of the parity generator
44	output OUT of the parity generator
46	clock input CL of the parity generator
48	input IN of the random-number register
50	output OUT of the random-number register
52	clock input CL of the random-number register
54	data bus
56	external reset signal (RESET)
58	external clock signal (EXTCLK)
60	reset inputs RES of the parity generator and the random-number register
Nosz	number of frequency oscillators
Nlog	number of logic operations for a parity formation
Nz	number of bits for a random number
Z	random number